7. An integrated circuit wafer comprising:

substrate comprising a wafer material, said substrate having first and second surfaces, said first surface having a circuit layer comprising integrated circuit elements constructed thereon;

Q3 a plurality of vias extending a first distance from said first surface of said substrate into said substrate, said vias comprising a stop layer comprising a stop material that is more resistant to chemical/mechanical polishing (CMP) than said wafer material;

a dielectric layer having top and bottom surfaces, said dielectric layer covering said circuit layer such that said bottom surface is in contact with said integrated circuit layer; and

a plurality of electrical conductors buried in said dielectric layer and making electrical connections to said integrated circuit elements.